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SUMMARY

Call For Tender IO/22/CFT/7-930/ERA

Central Interlock System – Fast Architecture Engineering and Development Framework Service Contract

Background

The ITER Interlock Control System (ICS) is the ITER Control System in charge of the implementation of the investment protection mechanisms at ITER through the automated execution of interlock functions. It is composed of the Central Interlock System (CIS), the Advanced Protection System (APS), both procured in-fund by IO (PBS.46), and of Plant Interlock Systems (PIS), provided by the different plant systems of ITER.

The CIS implements central interlock functions, which aim at the coordination and supervision of events generated by APS & PIS and of actions actuated by PIS. The different PIS are in charge of local protection functions with plant-specific interlock events or actions. local protection functions have transversal side-effects. The APS implements hybrid protection functions that concern integrated operation with or without plasma. Hybrid protection functions combine dynamic evaluation of the tokamak physical state-space with discrete logic such that events concerning integrated operation are detectable. Additionally, the APS is in charge of the main parts of the ITER disruption mitigation control path.

Concerning the above systems, an architecture composed of slow (PLC), fast (FPGA-based controllers) and hardwired technologies have been designed in adherence to the IEC-61508 standard.

The FPGA-based controllers are called CIS Fast Architecture (FA), which cover all subsystems of APS, Fast PIS (F-PIS), and some subsystems of CIS.

Purpose

This contract focuses on the CIS-FA. Its purpose allows an opportunity to participate in the design, development and V&V of CIS-FA subsystems as described in more detail below.

CIS Fast Architecture (FA) can be divided into two types of system;

1. The cRIO instrumented hosts, are combinations of PC-Host and National instrument cRIO FPGA connected via PCI Express. The FPGAs are tasked with executing pure logical functions, while interfacing through point-to-point 24V-industrial or 5V-TTL connections to PIS. The PC-Hosts are tasked with executing supporting functions like

configuration, status monitoring, logging state-changes to the CIS central logging system.
2. The cRIO instrumented CODAC interfaces, are cRIO instrumented hosts that can interface to the conventional ITER diagnostic and control systems through real-time Ethernet connections. A requirement for these systems is to isolate the central interlock functions from the conventional layer guaranteeing the performance of the interlock layer.

All CIS-FA developments utilise a real-time Linux kernel. The baselined FPGA device is the 14-slot National Instrument NI9159 cRIO, which contains a Xilinx Virtex-5. The host-side software includes a real-time application built on MARTe2 real-time framework and components. The host-side application interfaces to SCADA and central data-logging systems through OPC UA.

This framework-contract covers design, development and system V&V towards ITER First Plasma (FP) and Post-First Plasma Operation (PFPO-1), with the following branches of activities:

1. FP activities that concern design, development and system V&V for six sub-systems from CIS and APS.
2. FP activities that concern modification, retrofitting and system V&V of key CIS sub-systems;
3. PFPO-1 activities in support of design and prototyping for two sub-systems spanning the DMS-PIS.

The required services indicate a separation into two lots:

1. Overall system design, development, firmware integration & Validation and Verification.
2. Firmware design, development & Validation and Verification.

At a high level system design and development of CIS-FA systems follows the PCDH https://www.iter.org/mach/codac/PlantControlHandbook

The PCDH is expanded into design patterns, techniques and measures specific to CIS-FA which are internal IO documents.

Scope of work

The work shall be structured in individual task orders under the overall framework of the contract. Each task order shall focus on a specific system or submodules applicable to several subsystems. Additionally task-orders shall separate system development from system V&V depending on the criticality of the system such that each task-order can then be awarded to separate teams within one organisation or separate organisations in adherence to IEC61508 requirements.

The services to be requested in the task orders will cover the following:

- Engineering services covering the participation in the design, manufacturing, development, commissioning and testing of CIS-FA systems, prototypes, interfaces or library modules.
- Real-time C/C++ software development on Linux involving PCIe interfaces.
- Firmware integration through LabVIEW/FPGA of library modules based VHDL, Xilinx IP, LabVIEW/FPGA VIs, TCL, or constraint files.
- Support IO in the preparation of the system engineering dossiers; requirements, designs, V&V plans, V&V procedures, integration & operation manuals.
- Software V&V involving code reviews, static analysis, unit-testing, integration testing and end-to-end system testing.
- FPGA firmware V&V involving code reviews, static analysis, and simulations at functional, gate and post-PaR level using SystemVerilog. Firmware V&V also involves Timing constraints and Design Rules Check report reviews.

The work shall be performed at the company's premises and partially on the ITER site as specified by particular task-orders.

Contract schedule

The Contract is scheduled to come into force in September 2023 for a duration of four (4) years, with the possibility of the extension of an additional year.

Procurement timetable

The tentative timetable is as follows:

Call for Nomination Release	t_0	January 2023
Receipt of Nominations	$t_1 = t_0 + 4$ weeks	
Issuance of Prequalification Application	$t_2 = t_1 + 4$ weeks	
Receipt of Prequalification Application	$t_3 = t_2 + 3$ weeks	
Notification of Prequalification Results	$t_4 = t_3 + 5$ weeks	
Issuance of Call for Tender	$t_5 = t_4 + 2$ weeks	
Tender Proposals Due Date:	$t_6 = t_5 + 9$ weeks	
Estimated Contract Award Date:	$t_7 = t_6 + 7$ weeks	
Estimated Contract Start Date:	$t_8 = t_7 + 2$ weeks	

Experience

The company's experience shall cover a broad range of capabilities as listed below:

- Design, construction and operation of instrumented safety systems for large heterogeneous facilities.
- Hardware and software design and integration of safety industrial control systems, under the IEC-61508 and IEC-61511 standards.
- Failure-mode assessment of heterogeneous I&C systems.
- Development of real-time systems in C/C++ for the Linux operating system, EPICS control system, CODAC software framework and database management.
- Development of software and prototypes under National Instruments cRIO platform and LabView, Xilinx ISE.
- Specific experience with Linux device drivers for PCIe.
- C/C++ software Validation and Verification.
- FPGA firmware Validation and Verification.
- Review of I&C cabling diagrams under French standard NFC-15-100.
- Clear, precise, unambiguous documentation writing in English and open reporting culture.

Candidature

Participation is open to all legal persons participating either individually or in a grouping (consortium). All legal persons including all consortium members should be established in an ITER Member State. A legal person cannot participate individually or as a consortium partner in more than one application or tender. A consortium may be a permanent, legally-established grouping or a grouping which has been constituted informally for a specific tender procedure. All members of a consortium (i.e. the leader and all other members) are jointly and severally liable to the ITER Organization. The consortium cannot be modified later without the approval of the ITER Organization.

Legal entities belonging to the same legal grouping are allowed to participate separately if they are able to demonstrate independent technical and financial capacities. Bidders' (individual or consortium) must comply with the selection criteria. IO reserves the right to disregard duplicated references and may exclude such legal entities form the tender procedure.

References

Further information on the ITER Organization procurement can be found at:
https://www.iter.org/proc/generalinfo.